REMARKS

In response to the Office Action mailed April 25, 2003, Applicants respectfully request that the Examiner reconsider his rejection of the specification, drawings and remaining claims.

In the specification, the paragraphs [0001] – [0003] have been amended to provide only recently available information, namely the serial numbers of co-pending applications.

The drawings stand objected to under 37 C.F.R. 1.83(a) on the grounds that FIGURES 1-26 generally lack formality and particularly that FIGURES 2-4 and 31 contain unlabeled blocks that should be labeled according to their functions. All drawings currently being amended are shown with deletions struckthrough and additions indicated in red on the sheets attached for the convenience of the Examiner. Attached are replacement sheets that include the proposed changes.

Claims 1-20 remain in this application.

Claims 1, 2, 4-6, 8, 10-11, and 17 have been amended.

Claims 7, 9, and 21 have been cancelled

Claims 2, 4 - 5, and 10 stand objected to because the claim language "can" and "can be" are not positive recitations of the invention. Claims 2, 4 – 5 and 10 have been amended to positively recite the corresponding structures and/or functions.

Claims 7 and 9 stand objected because " an input port on the IC for receiving difference programs" is not clearly described in the specification. Claims 7 and 9 have been cancelled.

Claim 11 stands objected to because the language "the circuitry" lacks antecedent basis. Claim 11 has been appropriately amended to provide the required antecedent basis for the structure "the circuitry".

Claim 5 stands objected to because the term "rate" has not been sufficiently defined. Applicants have amended Claim 5 to particularly point out that the "rate" being claimed is the "sampling rate." The term "sampling rate" is well known in the art of delta

sigma modulation.

Claim 15 stands objected to because the term "hybrid memory system" appears to the Examiner not to be clear in this claim. Applicants respectfully traverse this rejection. Specifically, Applicants respectfully notes that the hybrid memory system is described in FIGURES 30G1 and 30G2, which respectively show a delta sigma modulator implemented using a random access memory (RAM) and a series of corresponding memory manipulation instructions.

Claim 17 has been amended to depend from Claim 11 such that the claim language "said at least one control signal" has proper antecedent basis.

Claims 19-20 stand objected to because the claim language "two delta sigma modulators, each having an independent controllable output delay" finds no clear support in the specification. Applicants respectfully traverse this objection. In particular, Applicants respectfully call the Examiner's attention to delta sigma modulators 303a and 303b and delays 3040a and 3040b shown in FIGURE 30 of the present application. Textural support for the structures shown in FIGURE 30 is provided in paragraph [0099] of the present Detailed Description.

Claims 1-20 stand rejected under 35 U.S.C. §112, first paragraph because Claims 1, 4 – 6, prior to any amendment set forth above, are in "single means/step" claim format. The extent that these claims have not been amended above, Applicants respectfully traverse these rejections.

Applicants respectfully submit that the claims as they stood, before any amendments thereto, do not constitute "single means/step" claims, as defined 35 U.S.C. §112, as interpreted by the Courts.

A single means claim is a claim which merely recites one means plus a statement of function and nothing else. A means limitation is one which is expressed as a mean or step for performing a specific function without the recital of structure, material, or acts in support thereof. In *In Re Hyatt*, 708 F.2d 712 (1983) pg 712-715

Independent Claims 1, 4, 5, and 8, as originally filed, contained positive structural limitations. For example, Claim 1 as originally filed, is directed to a *modulator* for generating digital signals in response to programming, rather than simply "means" for generating digital signals. In other words, Claim 1 is not directed to merely "means" for generating digital signals in accordance to selectable programming.

The amendments set forth above adds additional structure to the claims, in view of the specification, to more particularly define the subject matter, which the applicant believes is the invention. In particular, Applicants have amended independent Claims 1, 4, 5, and 6 to particularly point out the feature that the modulator architecture is configurable by programming to support changes in architecture and/or order.

Claims 1-2, and 4-20 stand rejected under 35 U.S.C. §102(a), as being anticipated by *McGrath, et al. (*U.S. Patent No. 5,345,409) (hereinafter "the *McGrath* reference"). Applicants respectfully traverse these rejections.

The *McGrath* reference, does not teach a delta sigma modulator which is programmable, such that the topology and/or the modulator order can be configurable in response to at least one program to implement a corresponding one of the delta sigma algorithms. FIGURE 1 of the *McGrath* reference shows a set of delta sigma modulators 120 each having an analog input 5 and an output coupled to a corresponding set of decimation filters 130. The figures of the *McGrath* reference, and in particular FIGURE 1, do not disclose any control signal inputs allowing either for the reconfiguration of delta sigma modulators 120 architecturally or for a change in order of those modulators configurable in response to at least one program to implement a corresponding one of the delta sigma algorithms. Specifically, the *McGrath* reference does not disclose or suggest that a program, such as a microcode program, which allows for delta sigma modulators 120 to be selectively reconfigured. It appears from an examination of the textual portion of the *McGrath* reference that delta sigma modulators 120 are only conventional delta sigma modulators having a fixed order and a fixed architecture; delta sigma modulators 120 are only briefly described in the *McGrath* reference at Col. 10,

Lines 36-40, which includes no indication that these delta sigma modulators are configurable in response to at least one program to implement a corresponding one of the delta sigma algorithms.

Claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by *Keevill, et al. (*U.S. Patent No. 6,359,938) (hereinafter "the *Keevill* reference"). Applicants respectfully traverse these rejections.

Similar to the *McGrath* reference, the *Keevill* reference, discloses a sigma delta modulator in FIGURE 17 but only briefly mentions the characteristics of this delta sigma modulator at Col. 19, Lines 24 - 31. Specifically, the *Keevill* reference does not describe the delta sigma modulator shown in FIGURE 17 as having a configurable architecture and/or a variable order configurable in response to at least one program to implement a corresponding one of the delta sigma algorithms. FIGURE 17 appears to only show a fixed configuration delta sigma modulator with a single input and a single output, and no configuration control input or port. The text of the *Keevill* reference is also silent on the feature of programmability.

Claims 1-2, 4-9, 11-13 and 15-20 stand rejected under 35 U.S.C. §102(e), as being anticipated by *Engeler* (U.S. Patent No. 5,151,970) (hereinafter "the *Engeler* reference). Applicants respectfully traverse these rejections.

FIGURE 19 of the *Engeler* reference discloses a neural network system which includes an array of m number of analog-to-digital converters 110. Converter array 110 is textually described at Col. 21, Line 61- Col. 22, Line 29, which states that the analog-to-digital converters in array 110 are preferrably sigma delta type converters. However, other than a brief indication that the converters of array 110 are preferably sigma delta converters, there is no teaching as to either the specific architecture of those sigma delta converters, including the order of that architecture or the data rate through each data converter. Specifically, the *Engeler* reference does not teach that either the architecture, sampling rate, or order of the delta sigma data converters of block 110 of FIGURE 19 are programmable or otherwise reconfigurable, as required by the present

claims.

Claim 5 stands rejected under 35 U.S.C. §102(e) as being anticipated by *Del Signore, et al.* (U.S. Patent No. 5,157,395) (hereinafter "the *Del Signore* reference). Applicants respectfully traverse these rejections.

The *Del Signore* reference includes a delta sigma modulator 10 at the input of the analog to digital converter. The particular architecture and order of delta sigma modulator 10 is not disclosed. In particular, there is no indication, and *Del Signore* does not teach that either the order, architecture, or sampling rate of delta sigma modulator 10 is variable under programming control, as required by the claims of the present application.

No new matter has been added. The claims are merely amended to more particularly point out and distinctly claim the subject matter Applicants believe is inventive. Reconsideration and allowance of claims is now respectfully requested.

With the addition of no new claims, no additional filing fees are due. However, Applicants respectfully request a One Month Extension of Time to File Response as attached PTO/SB/22 with Extension Fees in the amount of $110.00 as reflected on the PTO/SB/17 Fee Transmittal. Also, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account Number 23-2426 of WINSTEAD SECHREST & MINICK P.C.

If the Examiner has any questions or comments concerning this paper or the present application in general, the Examiner is invited to call the undersigned at (214) 745-5374.

Respectfully submitted,
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Dated: September 16, 2003

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ANNOTATED SHEET SHOWING CHANGES:

Figure 2

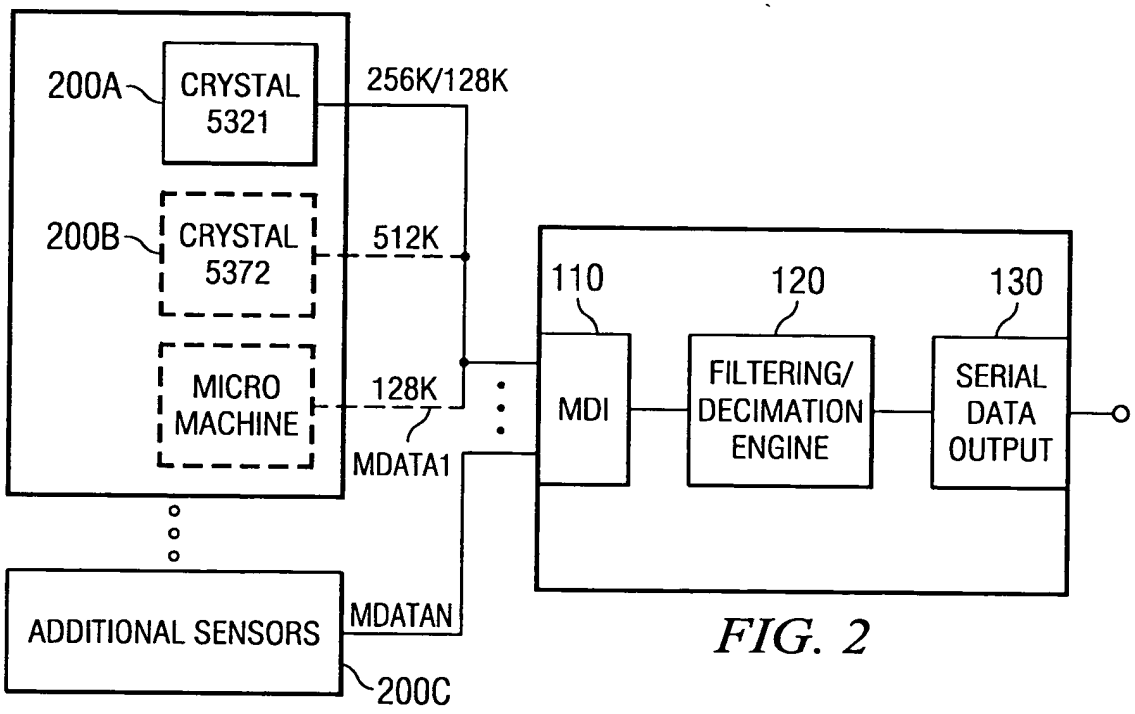

FIG. 2

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ANNOTATED SHEET SHOWING CHANGES:

Figure 3

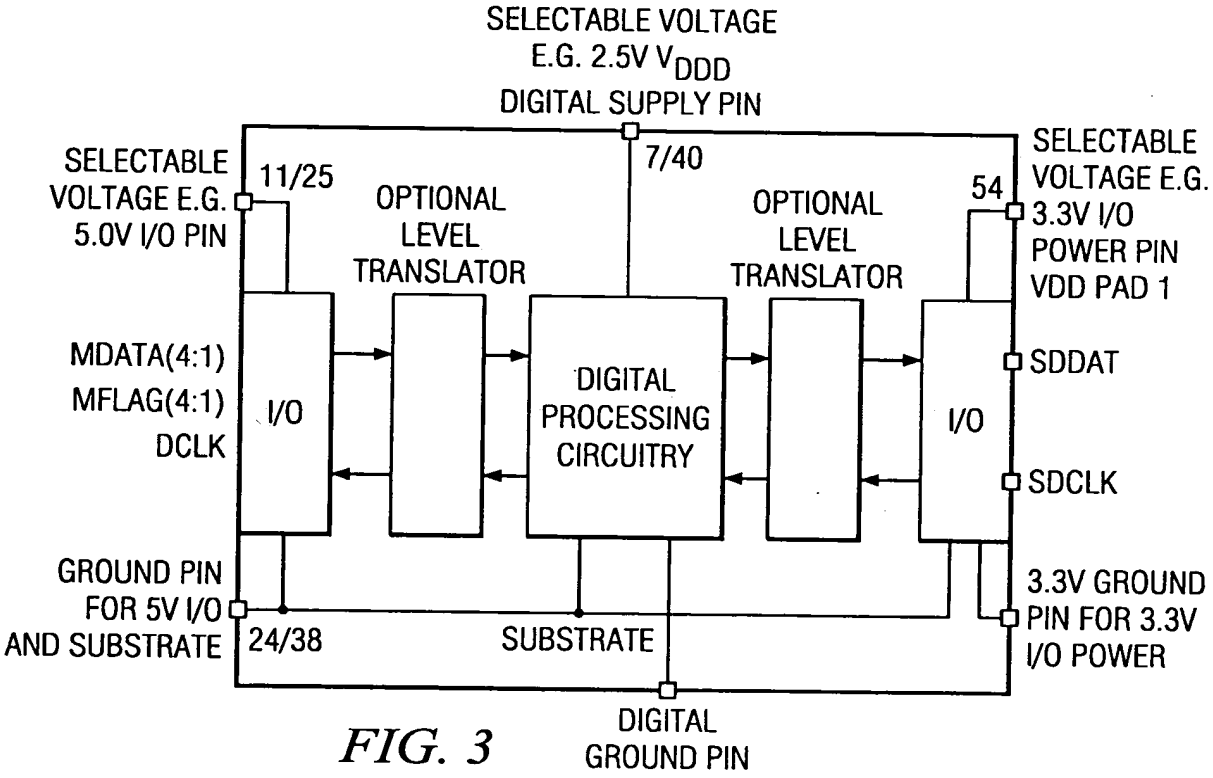

FIG. 3

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ANNOTATED SHEET SHOWING CHANGES:

Figure 4

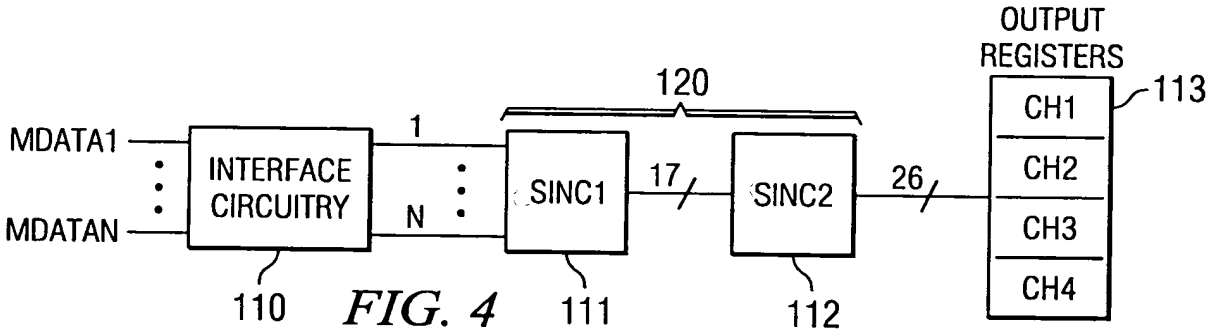

FIG. 4

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ANNOTATED SHEET SHOWING CHANGES:

Figure 31

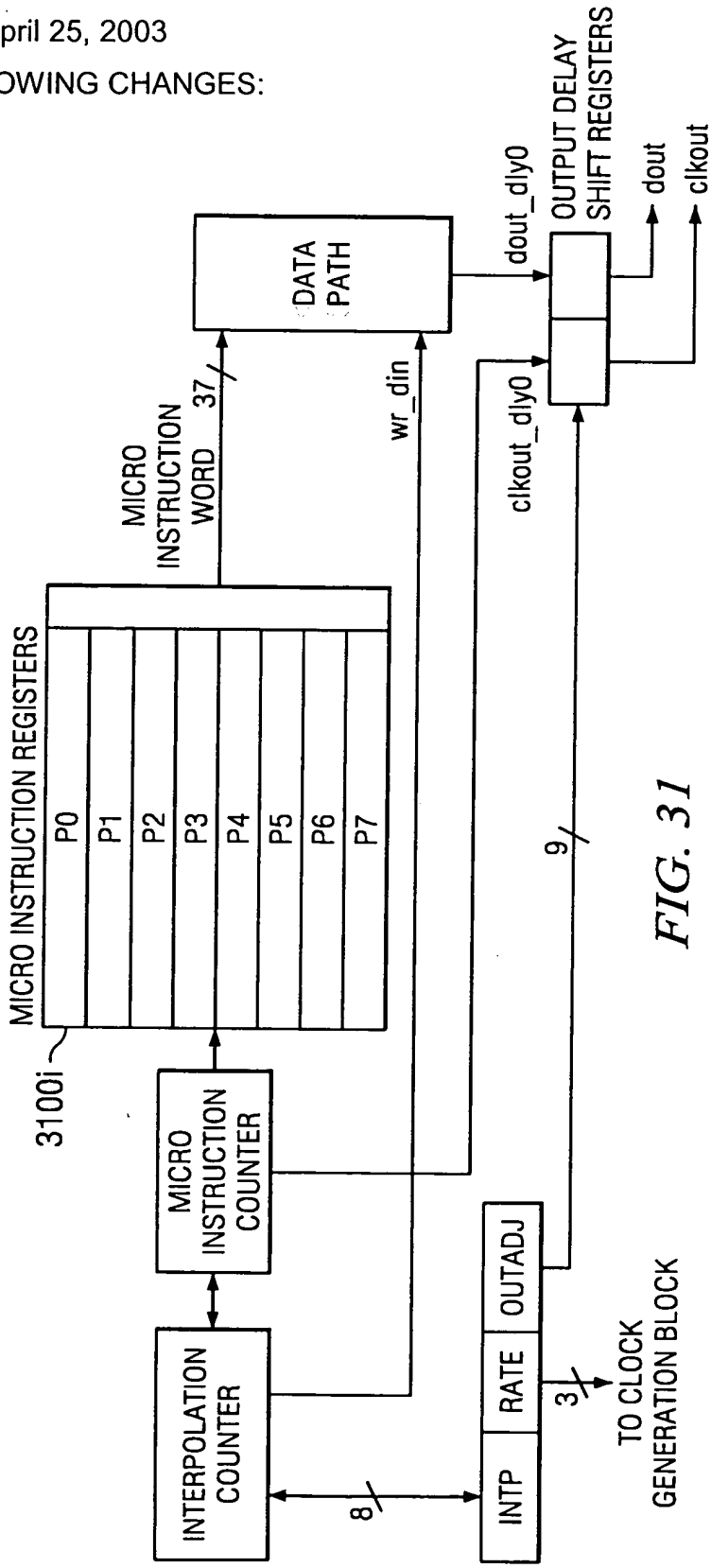

FIG. 31

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